

## **Training Schedule**

### **Week 1:**

#### **1) Introduction to VLSI and Digital Design Basics**

- . Basics of Digital Logic Design
- . Introduction to VLSI Chip Design and Design Methodologies

#### **2) VHDL/ Verilog and Basic CMOS Technology**

- . Introduction to VHDL/Verilog for VLSI Design
- . Basics of CMOS Technology
- . CMOS Layout Design Fundamentals
- . Lab Sessions on VHDL/Verilog and CMOS Basics

#### **3) Combinational Logic and Sequential Logic Design**

- . Combinational Logic Design
- . Sequential Logic Design
- . Lab Sessions on Combinational and Sequential Design

### **Week 2:**

#### **4) VLSI CAD Tools and RTL Design**

- . Introduction to VLSI CAD Tools
- . Register Transfer Level (RTL) Design
- . Hands-on Lab with CAD Tools and RTL Design

#### **5) Physical Design and Testing Techniques**

- . Introduction to VLSI Physical Design
- . Testing and Debugging in VLSI
- . Lab Sessions on Physical Design and Testing

#### **6) Specialized Topics and Final Project**

- . Low-Power Techniques in VLSI
- . Introduction to ASIC and FPGA Design

### **Course Summary**

At the end of the course, students will be able:

- . To understand VLSI and Digital Design
- . To understand about vulnerabilities in existing networking infrastructure.
- . Learning and understanding of VLSI tools, practical hands-on experience.
- . To understand physical design and testing techniques.